

High Speed, Low Power Wide Supply Range Amplifier

AD817

FEATURES
Low Cost
High Speed
- **50 MHz Unity Gain Bandwidth**
- **350 V/μs Slew Rate**
- **45 ns Settling Time to 0.1% (10 V Step)**

Flexible Power Supply
- **Specified for Single (+5 V) and Dual (±5 V to ±15 V) Power Supplies**
- **Low Power: 7.5 mA max Supply Current**

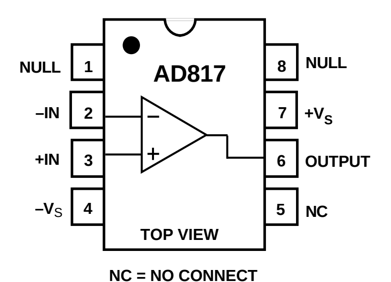
High Output Drive Capability
- **Drives Unlimited Capacitive Load**
- **50 mA Minimum Output Current**

Excellent Video Performance
- **70 MHz 0.1 dB Bandwidth (Gain = +1)**
- **0.04% & 0.08° Differential Gain & Phase Errors @ 3.58 MHz**

Available in 8-Pin SOIC and 8-Pin Plastic Mini-DIP

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD817 is a low cost, low power, single/dual supply, high speed op amp which is ideally suited for a broad spectrum of signal conditioning and data acquisition applications. This breakthrough product also features high output current drive capability and the ability to drive an unlimited capacitive load while still maintaining excellent signal integrity.

The 50 MHz unity gain bandwidth, 350 V/μs slew rate and settling time of 45 ns (0.1%) make possible the processing of high speed signals common to video and imaging systems. Furthermore, professional video performance is attained by offering differential gain & phase errors of 0.04% & 0.08° @ 3.58 MHz and 0.1 dB flatness to 70 MHz (gain = +1).

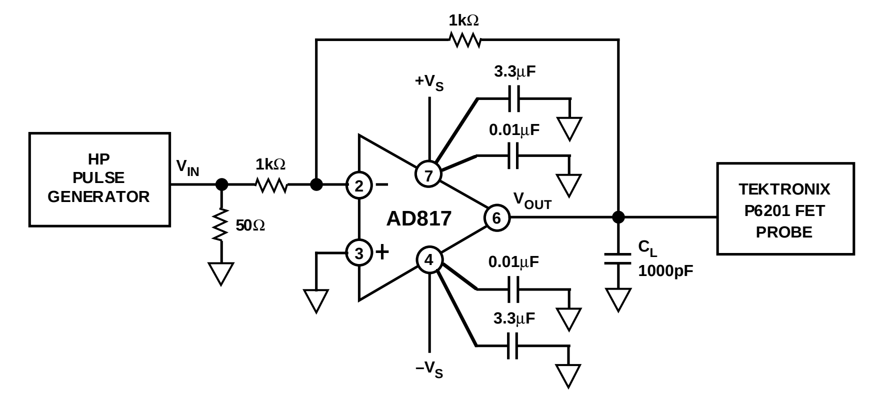
The AD817 is fully specified for operation with a single +5 V power supply and with dual supplies from ±5 V to ±15 V. This power supply flexibility, coupled with a very low supply current of 7.5 mA and excellent ac characteristics under all power supply conditions, make the AD817 the ideal choice for many demanding yet power sensitive applications.

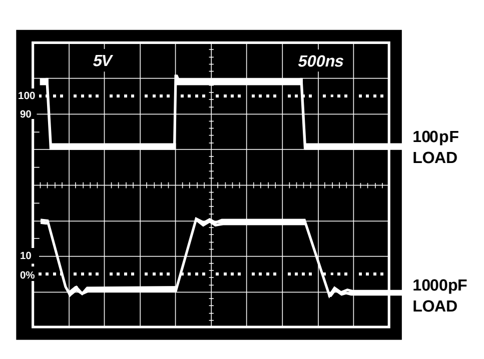
In applications such as ADC buffers and line drivers the AD817 simplifies the design task with its unique combination of a 50 mA minimum output current and the ability to drive unlimited capacitive loads.

The AD817 is available in 8-pin plastic mini-DIP and SOIC packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD817AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD817AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8





AD817 Driving a Large Capacitive Load

REV. B

One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD817–SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	AD817A Min	AD817A Typ	AD817A Max	Units
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V	30	35		MHz
		±15 V	45	50		MHz
		0, +5 V	25	29		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±5 V	18	30		MHz
		±15 V	40	70		MHz
		0, +5 V	10	20		MHz
Full Power Bandwidth[1]	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		15.9		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		5.6		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	200	250		V/µs
	Gain = 1	±15 V	300	350		V/µs
		0, +5 V	150	200		V/µs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V		45		ns
	0 V–10 V Step, A_V = –1	±15 V		45		ns
to 0.01%	–2.5 V to +2.5 V	±5 V		70		ns
	0 V–10 V Step, A_V = –1	±15 V		70		ns
Total Harmonic Distortion	F_C = 1 MHz	±15 V		63		dB
Differential Gain Error	NTSC	±15 V		0.04	0.08	%
(R_{LOAD} = 150 Ω)	Gain = +2	±5 V		0.05	0.1	%
		0, +5 V		0.11		%
Differential Phase Error	NTSC	±15 V		0.08	0.1	Degrees
(R_{LOAD} = 150 Ω)	Gain = +2	±5 V		0.06	0.1	Degrees
		0, +5 V		0.14		Degrees
INPUT OFFSET VOLTAGE		±5 V to ±15 V		0.5	2	mV
	T_{MIN} to T_{MAX}				3	mV
Offset Drift				10		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	6.6	µA
	T_{MIN}				10	µA
	T_{MAX}				4.4	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		25	200	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
OPEN LOOP GAIN	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		2	4		V/mV
	T_{MIN} to T_{MAX}		1.5			V/mV
	R_{LOAD} = 150 Ω		1.5	3		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		4	6		V/mV
	T_{MIN} to T_{MAX}		2.5	5		V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω					
	(50 mA Output)		2	4		V/mV
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5	78	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
		±15 V	80	100		dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		75	86		dB
	T_{MIN} to T_{MAX}		72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±5 V, ±15 V		15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz

Parameter	Conditions	V_S	AD817A Min	Typ	Max	Units
INPUT COMMON-MODE VOLTAGE RANGE		±5 V	+3.8	+4.3		V
			–2.7	–3.4		V
		±15 V	+13	+14.3		V
			–12	–13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
	R_{LOAD} = 500 Ω	0, +5 V	+1.5, +3.5			V
Output Current		±15 V	50			mA
		±5 V	50			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
INPUT RESISTANCE				300		kΩ
INPUT CAPACITANCE				1.5		pF
OUTPUT RESISTANCE	Open Loop			8		Ω
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current		±5 V		7.0	7.5	mA
	T_{MIN} to T_{MAX}	±5 V			7.5	mA
		±15 V			7.5	mA
	T_{MIN} to T_{MAX}	±15 V		7.0	7.5	mA

NOTES
[1]Full power bandwidth = slew rate/2 π V_{PEAK}.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . See Derating Curves
Small Outline (R) . . . . See Derating Curves
Input Voltage (Common Mode) . . . . $±V_S$
Differential Input Voltage . . . . ±6 V
Output Short Circuit Duration . . . . See Derating Curves
Storage Temperature Range N, R . . . .–65°C to +125°C
Operating Temperature Range . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air: 8-pin plastic package: θ_{JA} = 100°C/watt; 8-pin SOIC package: θ_{JA} = 160°C/watt.

Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD817 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



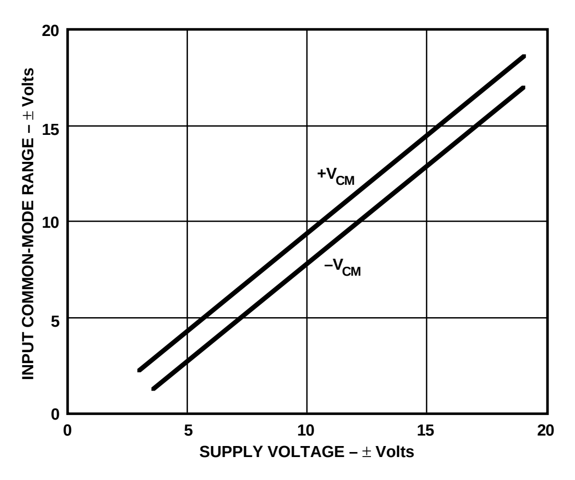


Figure 1. Common-Mode Voltage Range vs. Supply

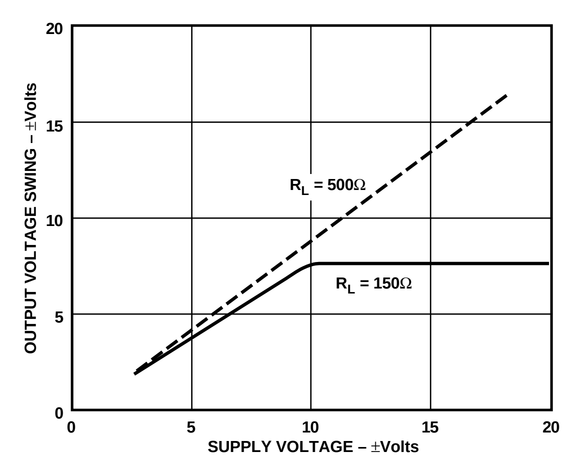


Figure 2. Output Voltage Swing vs. Supply

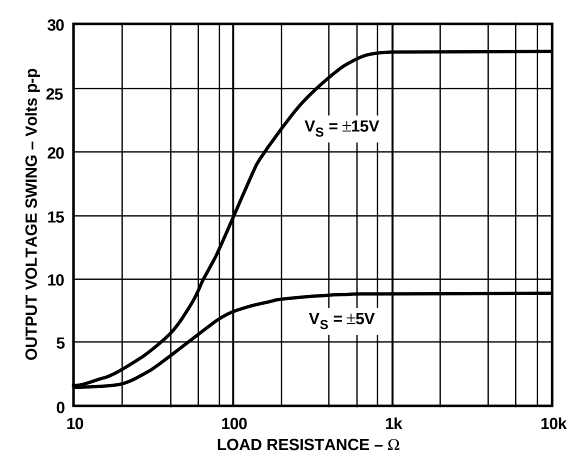


Figure 3. Output Voltage Swing vs. Load Resistance

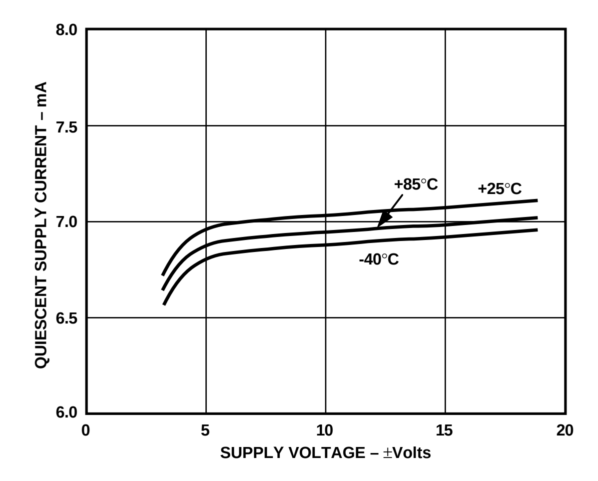


Figure 4. Quiescent Supply Current vs. Supply Voltage for Various Temperatures

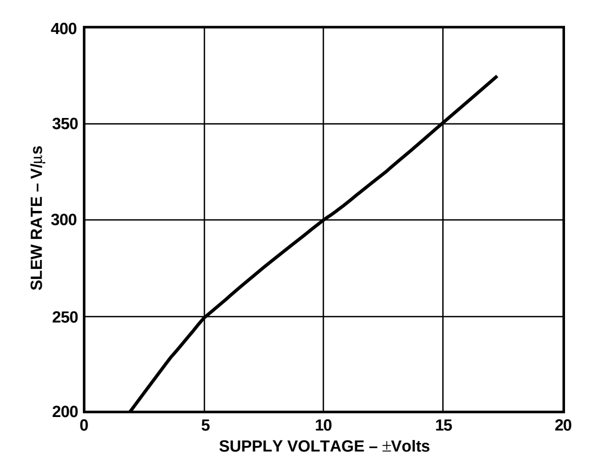


Figure 5. Slew Rate vs. Supply Voltage

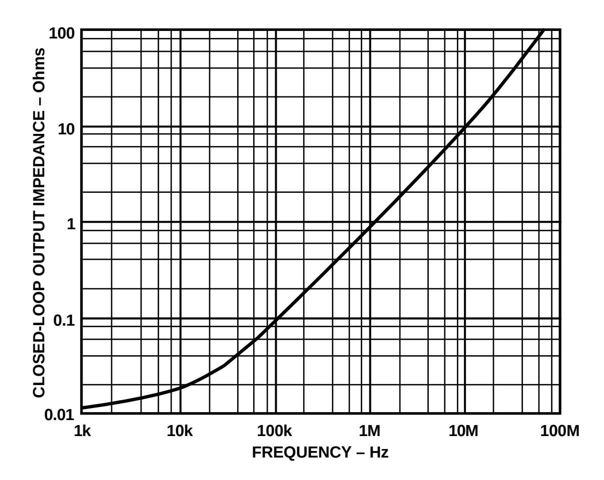


Figure 6. Closed-Loop Output Impedance vs. Frequency

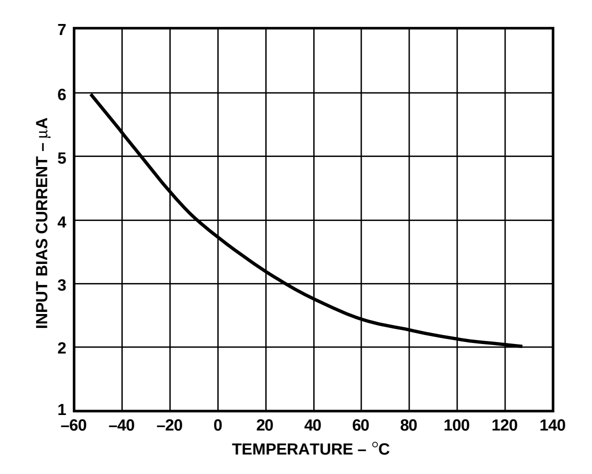


Figure 7. Input Bias Current vs. Temperature

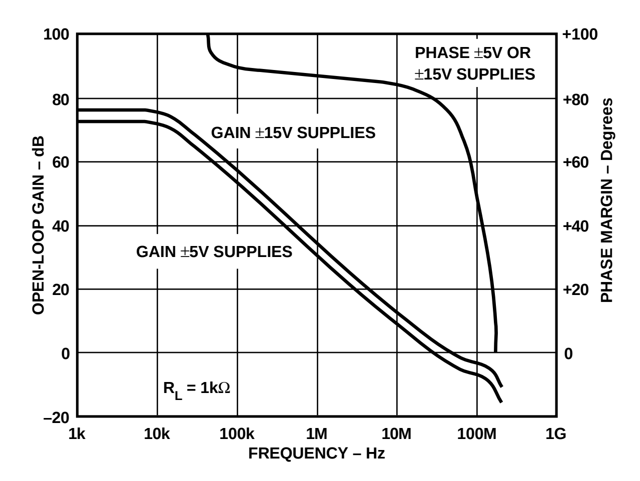


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

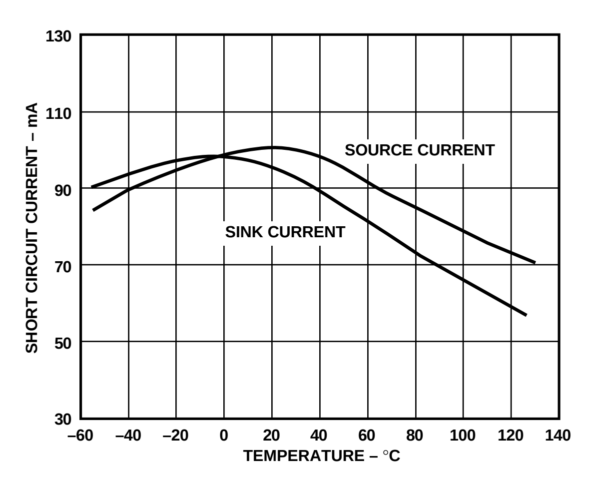


Figure 8. Short Circuit Current vs. Temperature

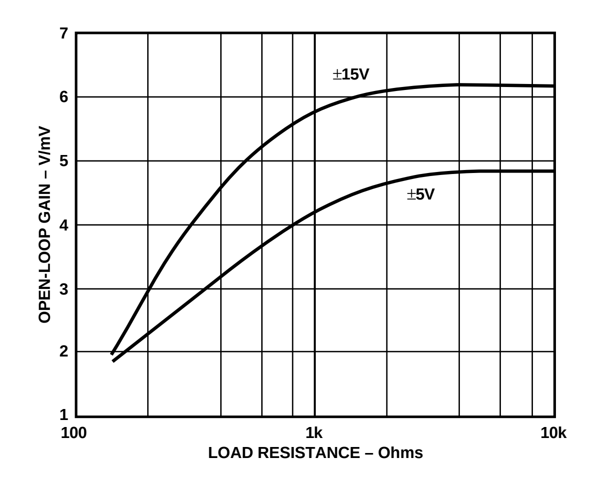


Figure 11. Open Loop Gain vs. Load Resistance

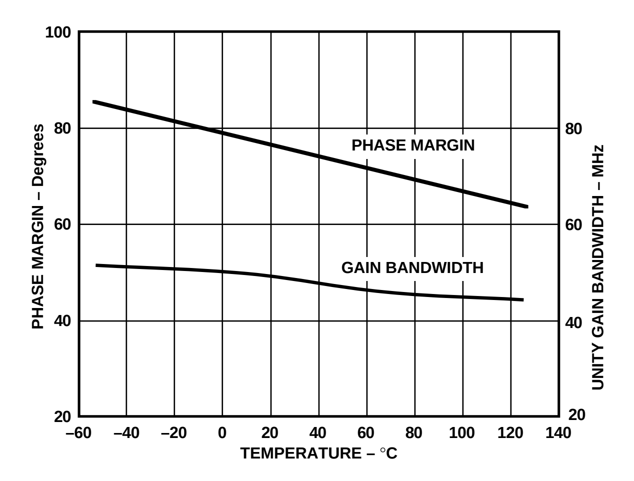


Figure 9. Unity Gain Bandwidth and Phase Margin vs. Temperature

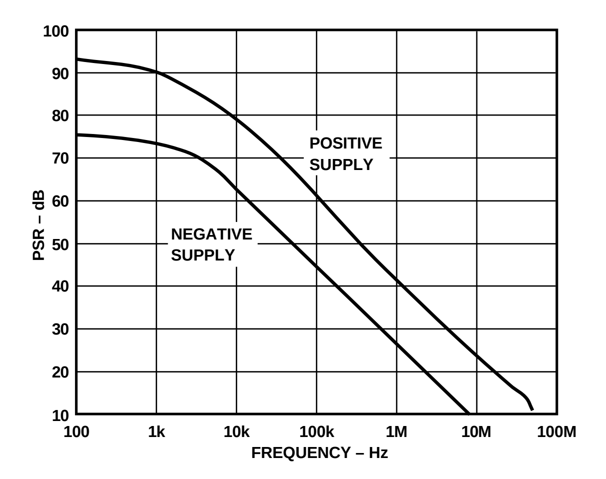


Figure 12. Power Supply Rejection vs. Frequency

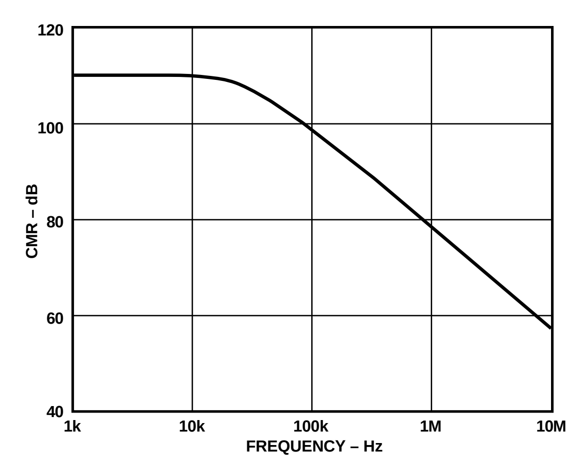


Figure 13. Common-Mode Rejection vs. Frequency

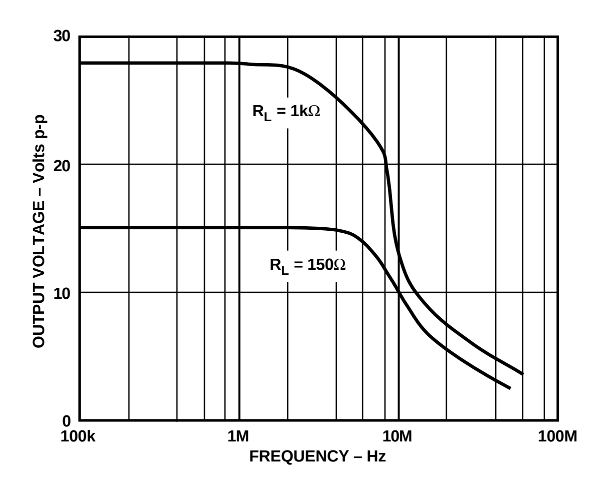


Figure 14. Large Signal Frequency Response

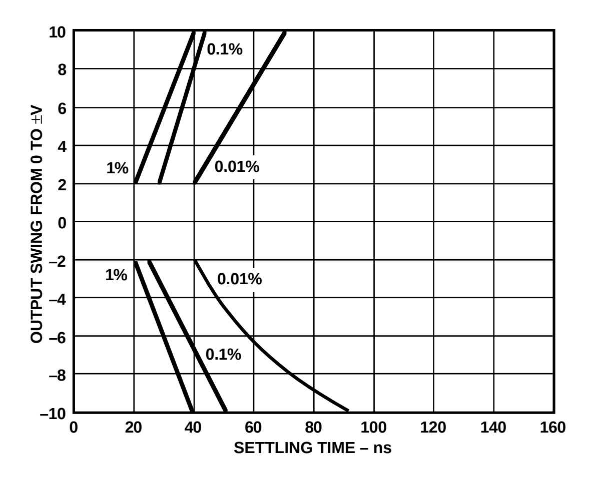


Figure 15. Output Swing and Error vs. Settling Time

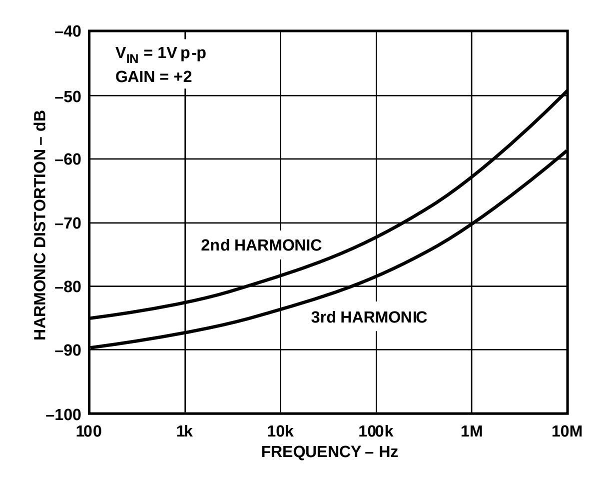


Figure 16. Harmonic Distortion vs. Frequency

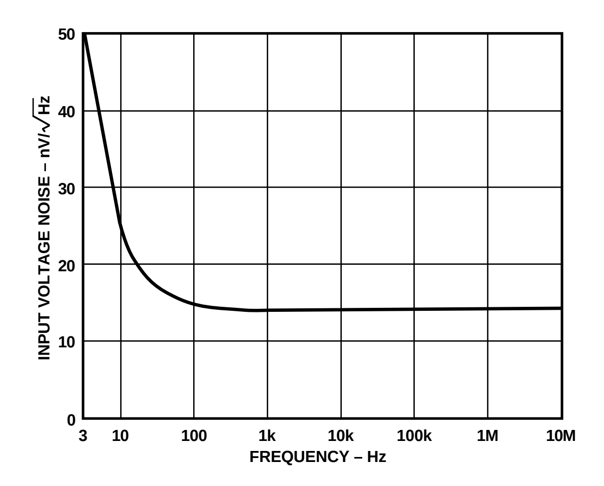


Figure 17. Input Voltage Noise Spectral Density

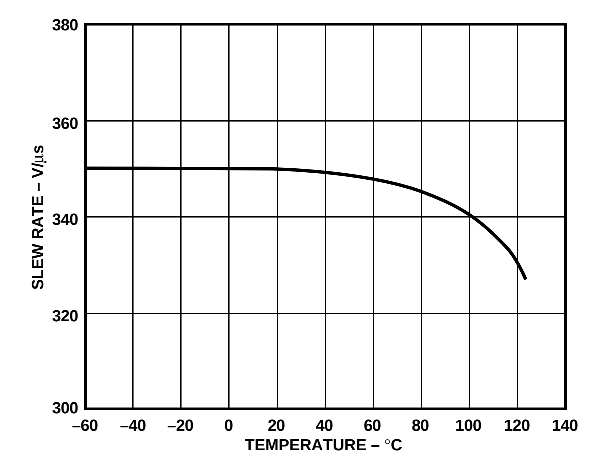


Figure 18. Slew Rate vs. Temperature

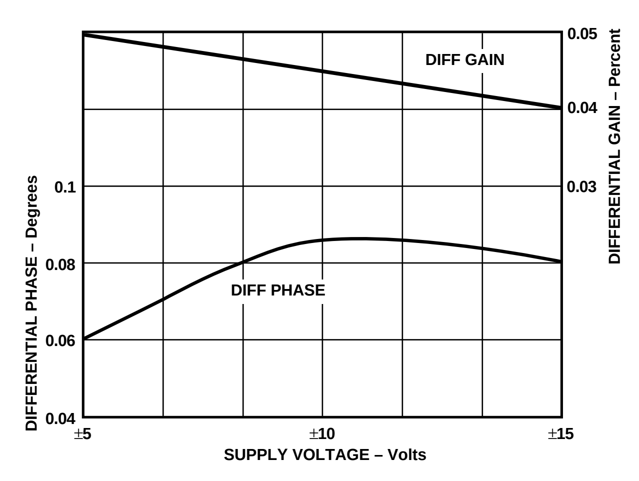


Figure 19. Differential Gain and Phase vs. Supply Voltage

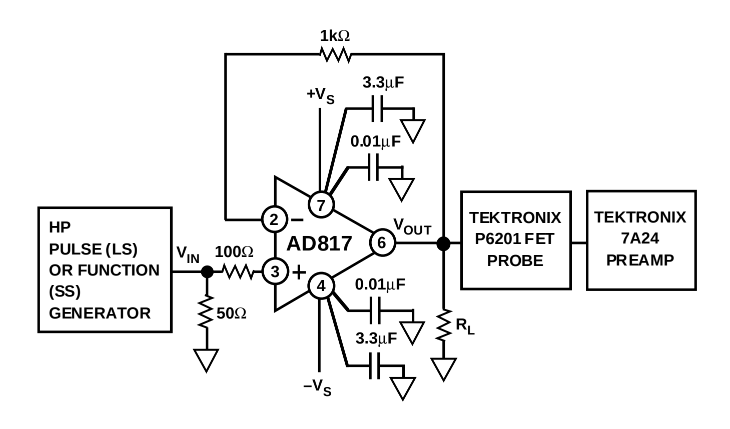


Figure 22. Noninverting Amplifier Connection

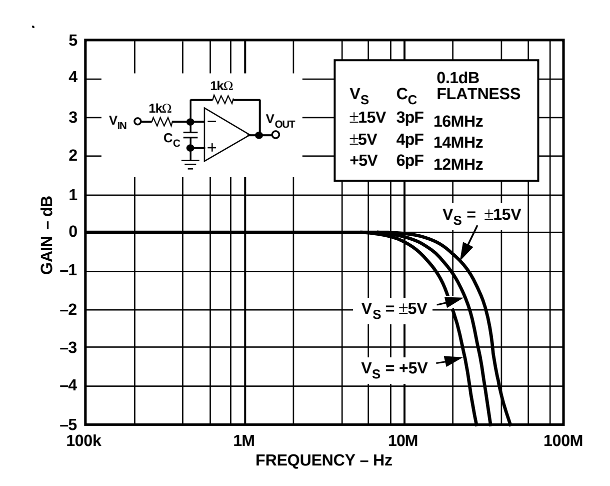


Figure 20. Closed-Loop Gain vs. Frequency, Gain = –1

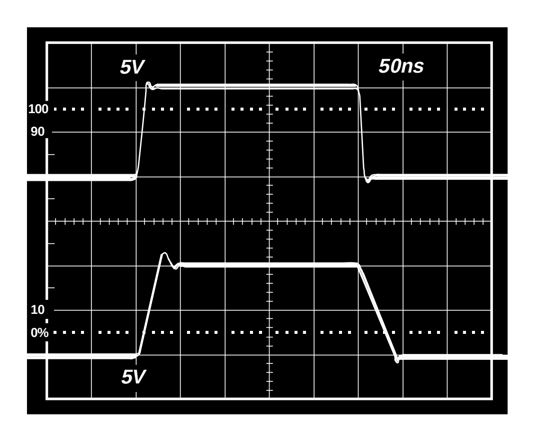


Figure 23. Noninverting Large Signal Pulse Response, R_L = 1 kΩ

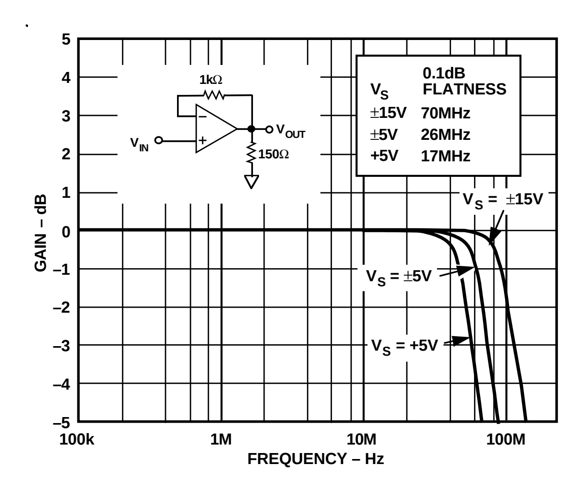


Figure 21. Closed-Loop Gain vs. Frequency, Gain = +1

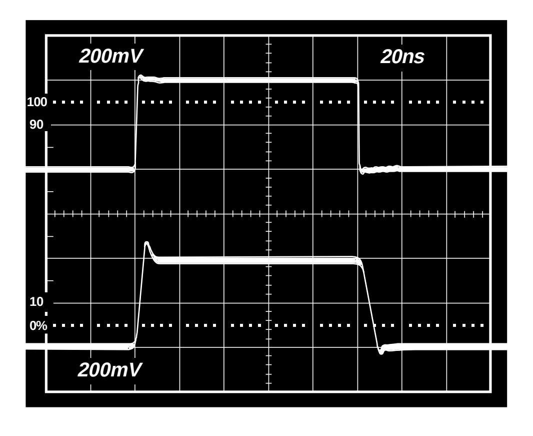


Figure 24. Noninverting Small Signal Pulse Response, R_L = 1 kΩ

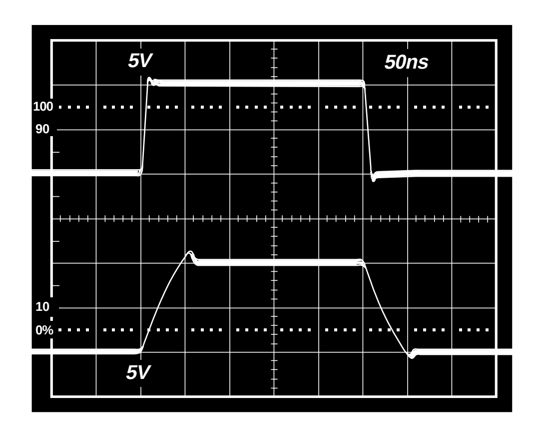


Figure 25. Noninverting Large Signal Pulse Response, R_L = 150 Ω

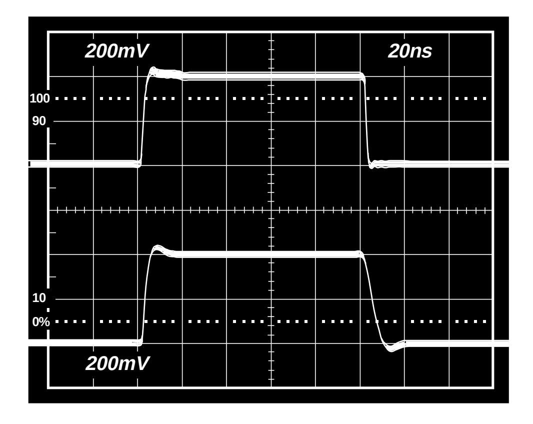


Figure 26. Noninverting Small Signal Pulse Response, R_L = 150 Ω

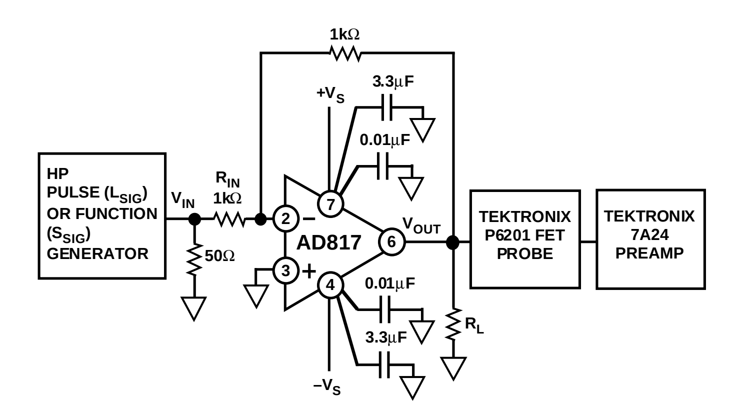


Figure 27. Inverting Amplifier Connection

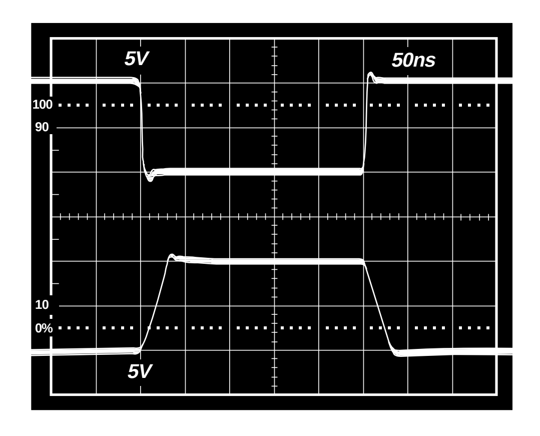


Figure 28. Inverting Large Signal Pulse Response, R_L = 1 kΩ

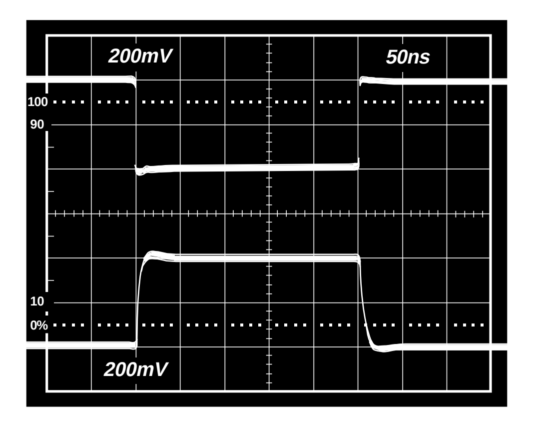


Figure 29. Inverting Small Signal Pulse Response, R_L = 1 kΩ

DRIVING CAPACITIVE LOADS

The internal compensation of the AD817, together with its high output current drive, permit excellent large signal performance while driving extremely high capacitive loads.

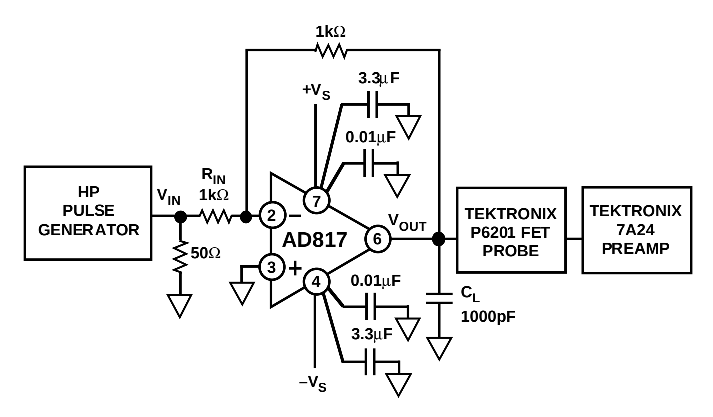


Figure 30a. Inverting Amplifier Driving a 1000 pF Capacitive Load

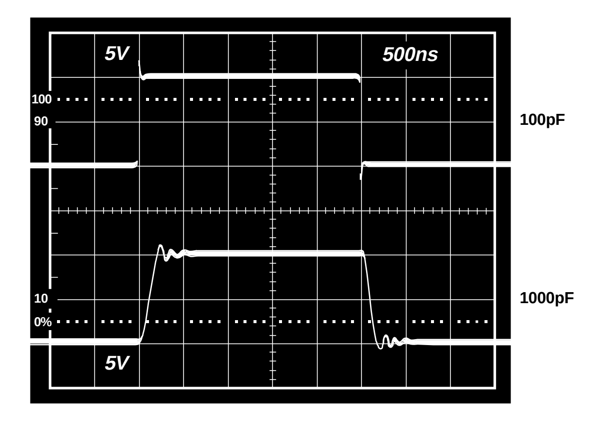


Figure 30b. Inverting Amplifier Pulse Response While Driving Capacitive Loads

THEORY OF OPERATION

The AD817 is a low cost, wide band, high performance operational amplifier which effectively drives heavy capacitive or resistive loads. It also provides a constant slew rate, bandwidth and settling time over its entire specified temperature range.

The AD817 (Figure 31) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies, and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C_F is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Effectively, some fraction of C_F contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining the stability of the amplifier.

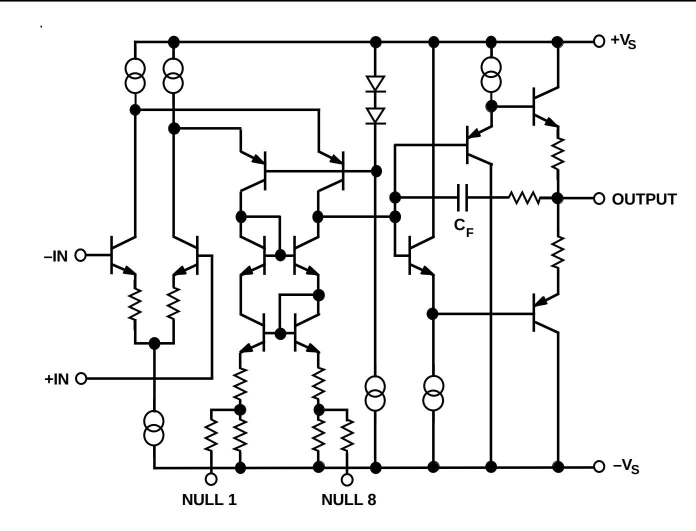


Figure 31. Simplified Schematic

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in Figure 22) is required in circuits where the input to the AD817 will be subjected to transient or continuous overload voltages exceeding the +6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

GROUNDING & BYPASSING

When designing high frequency circuits, some special precautions are in order. Circuits must be built with short interconnect leads. When wiring components, care should be taken to provide a low resistance, low inductance path to ground. Sockets should be avoided, since their increased interlead capacitance can degrade circuit bandwidth.

Feedback resistors should be of low enough value (<1 kΩ) to assure that the time constant formed with the inherent stray capacitance at the amplifier's summing junction will not limit performance. This parasitic capacitance, along with the parallel resistance of R_F/R_{IN}, form a pole in the loop transmission which may result in peaking. A small capacitance (1 pF–5 pF) may be used in parallel with the feedback resistor to neutralize this effect.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. Ceramic disc capacitors of 0.1 µF are recommended.

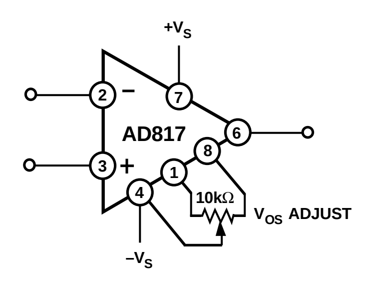


Figure 32. Offset Null Configuration

OFFSET NULLING

The input offset voltage of the AD817 is inherently very low. However, if additional nulling is required, the circuit shown in Figure 32 can be used. The null range of the AD817 in this configuration is ±15 mV.

AD817 SETTLING TIME

Settling time is comprised primarily of two regions. The first is the slew time in which the amplifier is overdriven, where the output voltage rate of change is at its maximum. The second is the linear time period required for the amplifier to settle to within a specified percent of the final value.

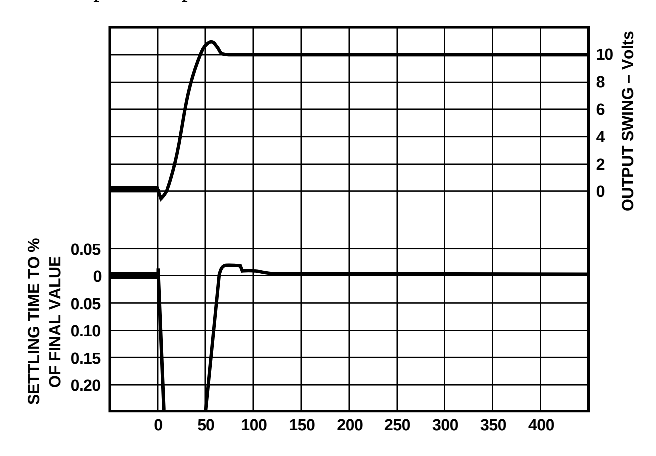


Figure 33. Settling Time in ns 0 V to +10 V

Measuring the rapid settling time of AD817 (45 ns to 0.1% and 70 ns to 0.01%–10 V step) requires applying an input pulse with a very fast edge and an extremely flat top. With the AD817 configured in a gain of –1, a clamped false summing junction responds when the output error is within the sum of two diode voltages (ª1 volt). The signal is then amplified 20 times by a clamped amplifier whose output is connected directly to a sampling oscilloscope. Figures 33 and 34 show the settling time of the AD817, with a 10 volt step applied.

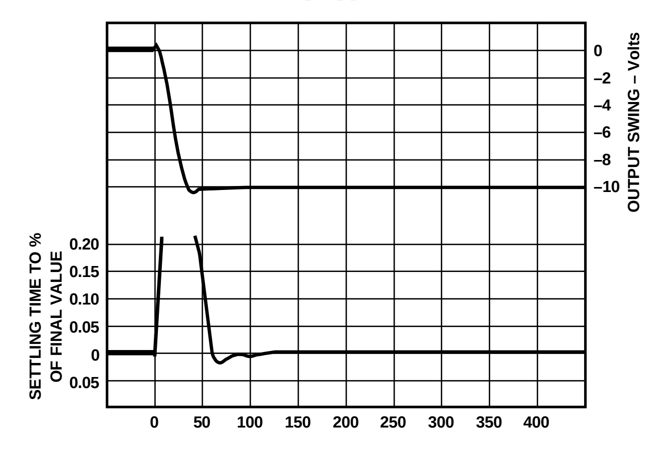


Figure 34. Settling Time in ns 0 V to –10 V

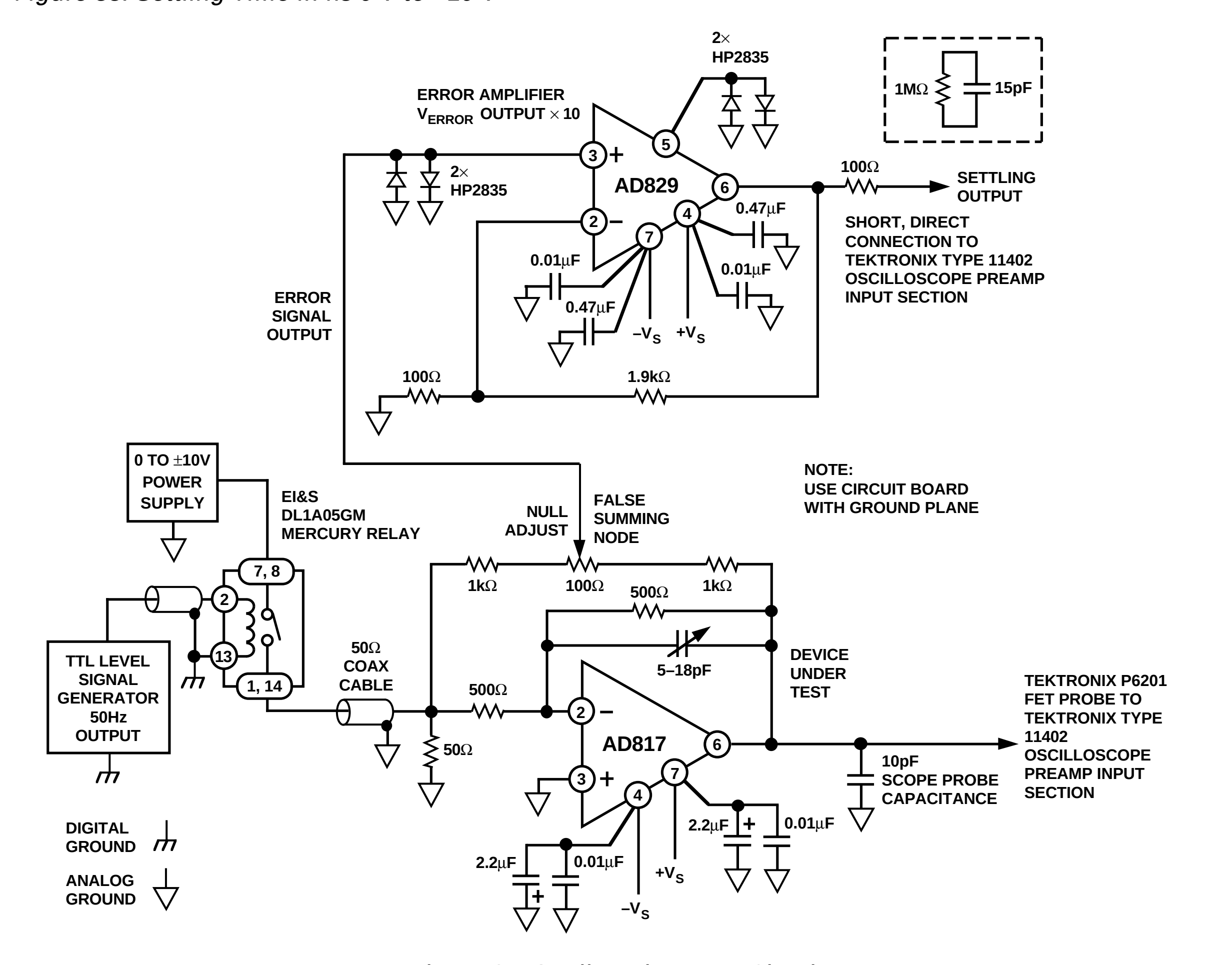


Figure 35. Settling Time Test Circuit

A HIGH PERFORMANCE ADC INPUT BUFFER

High performance analog to digital converters (ADCs) require input buffers with correspondingly high bandwidths and very low levels of distortion. Typical requirements include distortion levels of –60 dB to –70 dB for a 1 volt p-p signal and bandwidths of 10 MHz or more. In addition, an ADC buffer may need to drive very large capacitive loads.

The circuit of Figure 36 is useful for driving high speed converters such as the differential input of the AD733, 10-bit ADC. This circuit may be used with other converters with only minor modifications. Using the AD817 provides the user with the option of either operating the buffer in differential mode or from a single +5 volt supply. Operating from a +5 volt power supply helps to avoid overdriving the ADC—a common problem with buffers operating at higher supply voltages.

SINGLE SUPPLY OPERATION

Another exciting feature of the AD817 is its ability to perform well in a single supply configuration. The AD817 is ideally suited for applications that require low power dissipation and high output current and those which need to drive large capacitive loads, such as high speed buffering and instrumentation.

Referring to Figure 37, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: R1+ R3//R2 combine with C1 to form a low frequency corner of approximately 300 Hz.

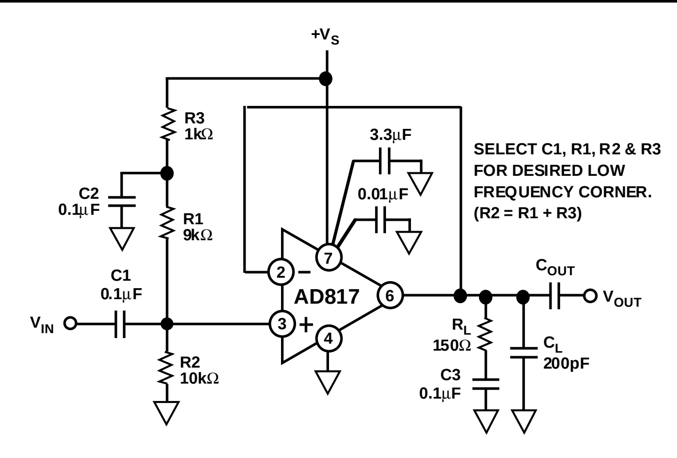


Figure 37. Single Supply Amplifier Configuration

Combining R3 with C2 forms a low-pass filter with a corner frequency of 1.5 kHz. This is needed to maintain amplifier PSRR, since the supply is connected to V_{IN} through the input divider. The values for R_L and C_L were chosen to demonstrate the AD817's exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, C3 was inserted in series with R_L.

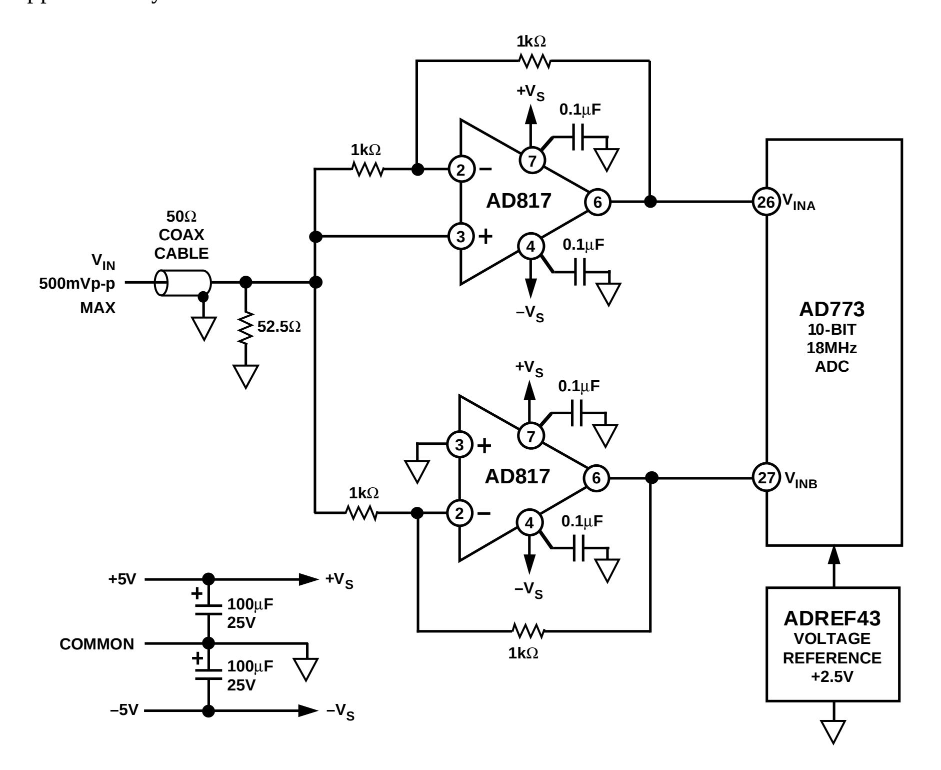


Figure 36. A Differential Input Buffer for High Bandwidth ADCs

HIGH SPEED DAC BUFFER

The wide bandwidth and fast settling time of the AD817 make it a very good output buffer for high speed current output D/A converters like the AD668. As shown in Figure 38, the op amp establishes a summing node at ground for the DAC output. The output voltage is determined by the amplifier's feedback resistor (10.24 V for a 1 kΩ resistor). Note that since the DAC generates a positive current to ground, the voltage at the amplifier output will be negative. A 100 Ω series resistor between the noninverting amplifier input and ground minimizes the offset effects of op amp input bias currents.

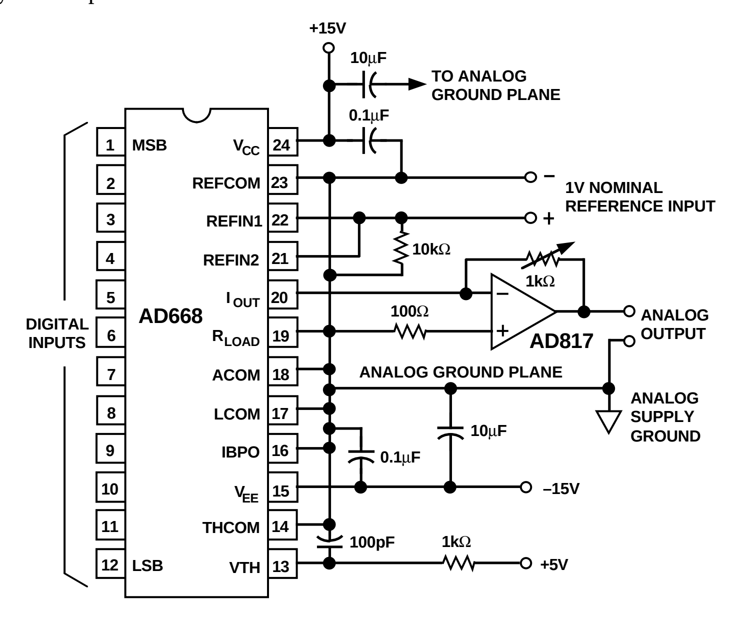
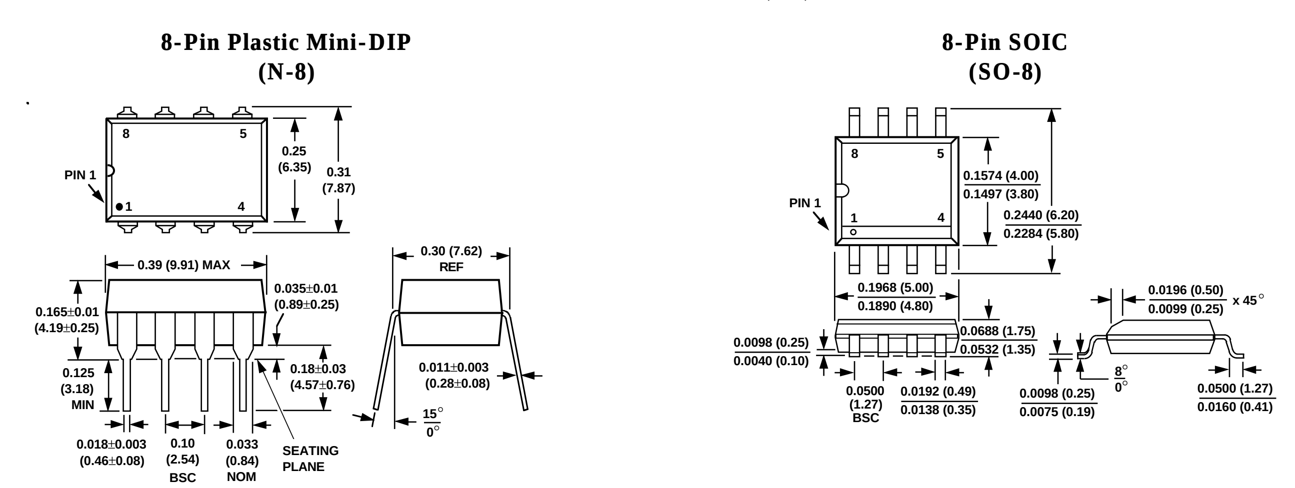


Figure 38. High Speed DAC Buffer

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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